Amendments to the Claims:

Please enter the amendments in the following listing of claims, wherein deletions are marked with strikethrough text and additions are marked with underlined text, and in which the amendments are made based on the assumption the amendments of the Amendment and Response of March 21, 2004 were entered:

1. (Presently Amended) A pixel display circuit comprising:

a pixel matrix, the pixel matrix having a first pixel component corresponding to a first color, a second pixel component corresponding to a second color, a third pixel component corresponding to a third color, a fourth pixel component corresponding to the first color, and a fifth pixel component corresponding to the second color, each of the first, second and third pixel components being coupled to a charge storage device and an associated switching device to control activation of each selection of the pixel components, each charge storage device of the first, second and third pixel components receiving a pulse from a previous line prior to activation of the associated switching device, each of the fourth and fifth pixel components being coupled to a charge storage device and an associated switching device to control activation of each selection of the pixel components, each charge storage device of the fourth and fifth pixel components coupled to ground.

2. (Presently Amended) The pixel display circuit of claim 1 in which the switch further comprises a transistor.

3. (Presently Amended) The pixel display circuit of claim 1 in which the switch further comprises a thin film transistor.

4. (Original) The pixel display circuit of claim 1 in which the charge storage device comprises a capacitor.

5. (Original) The pixel display circuit of claim 1 in which the charge storage device comprises a thin film capacitor.

6. (Original) The pixel display circuit of claim 1 in which the first color appears substantially red, the second color appears substantially green and the third color appears substantially blue.

7. (Presently Amended) The pixel display circuit of claim 1 in which each charge storage device of the first, second and third pixel components is fully charged prior to activation of the associated switching device.

8. (Previously Amended) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a computing device.

9. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a video signal.

10. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a television signal.

11. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a thin film emissive display device.

12. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a LCD display device.

13. (Presently Amended) An LCD pixel display having a plurality of pixels, each of the pixels having a first plurality of at least ~~five~~ three subpixel elements having paired gate lines, and having a second plurality of at least two subpixel elements, a representative subpixel element of the first plurality comprising:

a capacitor; the capacitor adapted to receive a first control signal; and a switch, the switch adapted to receive a second control signal, the switch being coupled to the capacitor and the switch being coupled to the subpixel element such that the capacitor receives the first control signal before the switch receives the second control signal;

and a representative subpixel element of the second plurality comprising:

a capacitor; the capacitor coupled to ground; and a switch, the switch adapted to receive the second control signal, the switch being coupled to the capacitor and the switch being coupled to the subpixel element.

14. (Original) The LCD pixel display of claim 14 wherein the first control signal causes a voltage to be applied to one electrode of the capacitor.

15. (Original) The LCD pixel display of claim 14 wherein the second control signal causes the switch to change an optical output associated with the subpixel element.

16. (Original) The LCD pixel display of 14 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a gate line and a data line such that control signals are transmitted to each switch via the gate line, and wherein the capacitor is coupled to a gate line associated with another pixel.

17. (Presently Amended) An LCD pixel display comprising:

a plurality of pixels, each pixel further comprising a first plurality of at least three ~~five~~ subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit wherein a first charging signal is applied prior to the releasing the sample and hold circuit;

each pixel further comprising a second plurality of at least two subpixels with an associated gate line, wherein each subpixel further includes a charge storage device coupled to ground and a switch coupled to the associated gate line.

18. (Original) The apparatus of claim 17 above wherein said sample and hold circuit comprises a capacitor transistor arrangement associated with each subpixel and wherein said transistor is timed to open after a previous signal is applied to said capacitor.

19. (Presently Amended) In a pixel array for an LCD display having a plurality of pixels each of said pixels having a group of subpixels, a first and second of said subpixels corresponding to a first color, a third subpixel corresponding to a second color and a fourth and fifth subpixel corresponding to a third color comprising:

a first means for switching associated with one of said first subpixel;

a second means for switching associated with the other of said second subpixel; a third means for switching associated with said third subpixel;

a fourth means for switching associated with said fourth subpixel,

a fifth means for switching associated with said fifth subpixel;

each of said first, second, third, fourth and fifth switching means having a corresponding means for storing a charge;

said switching means of the first, second and third subpixel being coupled to a gate line such that each of said switching means of the first, second and third subpixel is opened after each of said means for storing a charge is charged and in which the gate lines are paired;

the switching means of the fourth and fifth subpixel being coupled to a gate line and the storing means of the fourth and fifth subpixel being coupled to ground.

20. (Presently Amended) A method for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements having paired gate lines and having a second plurality of subpixel elements having a gate line and a ground line, with a capacitor of each subpixel element of the second plurality of subpixel elements coupled to ground, comprising ~~the steps of~~:

charging a capacitor with a first control signal; and

activating a transistor with a second control signal, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the first plurality of subpixel elements, such that the capacitor receives the first control signal before the switch receives the second control signal.

21. (Original) The LCD pixel display of claim 20 wherein the first control signal causes a voltage to be applied across the capacitor.

22. (Presently Amended) The LCD pixel display of claim 20 wherein the second control signal causes the transistor to change an optical output associated with one subpixel element of the ~~plurality of~~ subpixel elements.

23. (Original) The LCD pixel display of claim 20 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a gate line and a data line such that control signals are transmitted to each switch via the gate line, and wherein the capacitor of the first plurality of subelements is coupled to a gate line associated with another pixel.

24. (Original) The LCD pixel display of claim 20 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

25. (Presently Amended) A method for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements and a second plurality of subpixel elements, the LCD display being controlled substantially according to a clock signal, comprising ~~the steps of~~:

charging a capacitor with a first control signal during a first clock period, the first clock period occurring substantially immediately before a second clock period;

activating a transistor with a second control signal during the second clock period, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the subpixel elements of the first plurality of subpixel elements, the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the plurality of subpixel elements,

activating a transistor with the second control signal during the second clock period, the transistor being electrically coupled to a grounded capacitor, the grounded capacitor further coupled to ground, and the transistor being coupled to at least one of the subpixel elements of the second plurality of subpixel elements,

the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the plurality of subpixel elements,

transmitting an optical signal from the at least one optical output at least partially in response to the data signal.

26. (Original) The LCD pixel display of claim 25 wherein the first control signal causes a voltage to be applied across the capacitor.

27. (Presently Amended) The LCD pixel display of claim 25 wherein the second control signal causes the transistor to create a potentially visible optical output associated with one subpixel element of the first plurality of subpixel elements.

28. (Presently Amended) The LCD pixel display of claim 25 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a first gate line, a second gate line and a data line, such that the first control signal is received from the first control line coupled to the capacitor, the second control signal is received from the second control line ~~coupled to the transistor~~, and the data signal is received from the data line ~~coupled to the transistor~~.

29. (Original) The LCD pixel display of claim 25 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

30. (Presently Amended) An apparatus for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements having paired gate lines, comprising:

electrical means for charging a capacitor with a first control signal; and

control means for activating a transistor with a second control signal, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the plurality of subpixel elements, such that the capacitor receives the first control signal before the switch receives the second control signal;

each of the pixels of the plurality of pixels having a second plurality of subpixel elements, comprising:

a grounded capacitor coupled to ground; and

control means for activating a transistor with a second control signal, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the plurality of subpixel elements.

31. (Original) The apparatus of claim 30 wherein the electrical means causes a voltage to be applied across the capacitor.

32. (Presently Amended) The apparatus of claim 30 wherein the control means causes the transistor to change an optical output associated with one subpixel element of the first plurality of subpixel elements.

33. (Original) The apparatus of claim 30 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

34. (Presently Amended) An apparatus for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements and having a second plurality of subpixel elements, the LCD display being controlled substantially according to a clock signal, comprising ~~the steps of~~:

charging means for charging a capacitor with a first control signal during a first clock period, the first clock period occurring substantially immediately before a second clock period;

activating means for activating a transistor with a second control signal during the second clock period, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the first plurality of subpixel elements, the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the first plurality of subpixel elements,

the activating means further for activating a transistor with a second control signal during the second clock period, the transistor being electrically coupled to a grounded capacitor, the grounded capacitor being coupled to groung, and the transistor being coupled to at least one of the second plurality of

subpixel elements, the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the second plurality of subpixel elements,

light emitting means for transmitting an optical signal from the at least one optical output at least partially in response to the data signal.

35. (Original) The apparatus of claim 34 wherein the charging means causes a voltage to be applied across the capacitor.

36. (Presently Amended) The apparatus of claim 34 wherein the activating means causes the transistor to create a potentially visible optical output associated with one subpixel element of the first plurality of subpixel elements.

37. (Presently Amended) The apparatus of claim 34 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a first gate line, a second gate line and a data line, such that the first control signal is received from the first control line coupled to the capacitor, the second control signal is received from the second control line ~~coupled to the transistor~~, and the data signal is received from the data line ~~coupled to the transistor~~.

38. (Original) The apparatus of claim 34 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

39. (Presently Amended) An LCD pixel display having a plurality of pixels, each of the pixels having a first plurality of at least ~~five~~ three subpixel elements having paired gate lines and having a second plurality of at least two subpixel elements having, a representative subpixel element of the first plurality comprising:

a storage means; the storage means adapted to receive a first control signal; and

a switch means, the switch means adapted to receive a second control signal, the switch means coupled to the storage means and the switch means being coupled to the subpixel element such that the storage means receives the first control signal before the switch means receives the second control signal;

a representative subpixel element of the second plurality comprising:

a grounded storage means; the storage means coupled to ground; and

a switch means, the switch means adapted to receive a second control signal, the switch means coupled to the storage means and the switch means being coupled to the subpixel element.

40. (Original) The LCD pixel display of claim 39 wherein the first control signal causes a voltage to be applied to the storage means.

41. (Original) The LCD pixel display of claim 39 wherein the second control signal causes the switch means to change an optical output associated with the subpixel element.

42. (Original) The LCD pixel display of 39 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a gate line and a data line such that control signals are transmitted to the switch means via the gate line, and wherein the storage means is coupled to a gate line associated with another pixel.